# Rockchip RKNanoD Datasheet

**Revision 0.1**
**Jan. 2015**

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# Revision History

| Date | Revision | Description |
|---|---|---|
| 2015.01.26 | 0.1 | First release |
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# Chapter 1 Introduction

## 1.1 Overview

RKNanoD is a low-cost, low-power, high-efficiency digital multimedia chip which is based on ARM cortex-M3 processor architecture with Audio decoder hardware accelerator. It is designed for multimedia product and IOT applications.

By providing a complete set of peripheral interface, RKNanoD can support very flexible applications, including VOP, USB OTG, SD/MMC, I2C, I2S, SPI, PWM etc.

## 1.2 Features

### 1.2.1 Boot Option

- Boot from SDMMC Card
- Boot from eMMC flash
- Boot from SPI Nand/Nor flash
- Boot from USB

#### 1.2.2 Memory Organization

- 16KB boot ROM
- 64KB PMU SRAM for low power sleep mode
- 320KB IRAM and 256KB DRAM for core0 M3 sub-system
- 128KB IRAM and 256KB DRAM for core1 M3 sub-system
- 64KB/bank clock-gate control for reduce power consumption

#### 1.2.3 Processor

- Dual ARM Cortex-M3 core
  - A Thumb instruction set subset
  - Banked Stack Pointer (SP) only
  - Hardware divide instructions, SDIV and UDIV (Thumb 32-bit instructions)
  - Handler and Thread modes
  - Thumb and Debug states
  - Interruptible-continued LDM/STM, PUSH/POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
  - Support for ARMv6 unaligned accesses
- Nested Vectored Interrupt Controller (NVIC)
  - 32-level priority of interrupt
  - Dynamic reprioritization of interrupts
  - Priority grouping. This enables selection of pre-empting interrupt levels and non pre-empting interrupt levels
  - Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

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- Mail box
  - Support dual-core system: system core and calculation core
  - Support APB interface
  - Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Four interrupts to system core
  - Four interrupts to calculation core

### 1.2.4 Power Management Unit

- Multiple configurable work modes to save power by different frequency or automatically clock gating control or power domain on/off control
- 2 voltage domains and 3 separate power domains, which can be power up/down by software based on different application scenes

### 1.2.5 CRU (clock & reset unit)

- Support clock gating control for individual components
- One oscillator with 24MHz clock input and 1 embedded general purpose PLL
- Support global soft-reset control for whole SOC, also individual soft-reset for every components

### 1.2.6 Hardware Accelerator for Audio decode

- imdct36 calculation module
- sub-band synthesize module

### 1.2.7 Memory Interface

- SD/MMC controller
  - SD/MMC SPI mode/1bit mode/4bit mode
  - Support Multi Media Card Specification Version 4.41
  - Support SD Memory Card Specification Version 2.0
  - Cards Clock Rate up to PCLK, Re-scaling the SD/MMC clock (PCLK) with the 8-bits pre-scale register in SCU block
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
- eMMC Interface
  - Support MMC4.41 protocol
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - 8bits data bus width
- SFC Interface
  - Support transfer data from/to SPI flash device
  - Support x1,x2,x4 data bits mode
  - Support interrupt output, interrupt maskable

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- Support Spansion, MXIC,Gigadevice…vendor's nor flash memory

### 1.2.8 DISPLAY interface

- Support source data format: RGB565, YUV420
- Support UV swap
- Support YUV2RGB
- Support BT601 limited range
- Support BT709 limited range
- Support BT601 full range
- Support allegro dither down for RGB888 to RGB565
- Support RGB565 display data format
- Support display data swap
- Support max output resolution 400x400
- Built-in i8080 MCU interface
- Support EPD T-CON / E-INK

### 1.2.9 DMA Controller

- Two DMA Controllers in chip
  - DMAC1 Support 6 DMA channels
  - DMAC2 Support 2 DMA channels
  - Support incremental and fixed addressing mode
  - Support hardware and software trigger DMA transfer mode
  - Support error interrupt, transport-complete interrupt
  - When transport data is not align with source burst, the last data will be transported in single burst mode
  - Support LLP mode and auto-reload

### 1.2.10 USB interface

- USB 2.0 OTG controller and PHY
- Operates in High-Speed and Full-Speed mode
- Support Session Request Protocol(SRP) and Host Negotiation Protocol(HNP)
- Support 6 endpoints , one control endpoint, two IN/OUT endpoints, one IN endpoint
- Support 4 channels at Host mode, support bulk transfer

### 1.2.11 Low speed Peripheral interface

- I2C controller
  - Support 3 I2C controllers
  - Supports master modes of I2C bus
  - Software programmable clock frequency and transfer rate up to 100Kbit/s in standard mode or up to 400Kbit/s in Fast mode
  - Supports 7 bits and 10 bits addressing modes
- I2S
  - Support 2 I2S controllers
  - Support mono/stereo audio file
  - Support 16 ~ 32 bits audio data transfer

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- Support audio sample rate up to 192 KHz
- Support I2S, Left-Justified and Right-Justified digital serial data format

- PWM
  - 5 on-chip PWMs with interrupt-based operation
  - Programmable counter and duty cycle
  - Chained timer for long period purpose
  - Support single counter mode and reload mode
  - Configurable polarity
  - Support interrupt output
- SPI master
  - 2 on-chip SPIs
  - Serial-master operation – Enables serial communication with serial-slave peripheral devices
  - DMA Controller Interface – Enables interface to a DMA controller using a handshaking interface for transfer requests
  - Support interrupt interface to interrupt controller, and independently masking of interrupts
  - One hardware slave-select lines
  - Dynamic control of the serial bit rate of the data transfer
- GPIO
  - 3 groups of GPIO (GPIO0~GPIO2) , 32 GPIOs per group
  - All of GPIOs can be used to generate interrupt to CPU
  - All of pull-up GPIOs are software-programmable for pull-up resistor or not
  - All of pull-down GPIOs are software-programmable for pull-down resistor or not
  - All of GPIOs are always in input direction in default after power-on-reset
- Timer
  - 2 on-chip 64bits Timers in SoC with interrupt-based operation
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
- UART
  - 6 on-chip UARTs
  - AMBA APB interface
  - DMA Controller Interface – Enables interface to a DMA controller over the AMBA bus using a handshaking interface for transfer requests.
  - Support interrupt interface to interrupt controller.

### 1.2.12 Analog IP interface

- AUDIO-DAC
  - High Digital to Analog Convert SNR.
  - High Analog to Digital Convert SNR.
  - Differential analog input microphone input with boost pre-amplify and low-noise microphone bias.
  - Stereo line input.
  - Stereo line output.
  - PLL internal.

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- Stereo virtual-ground headphone amplify with ultra-low power.
- One 24bit/8k~192K I2S/PCM interface for stereo DAC and ADC.
- ALC (Automatic Level Control) in ADC path and DRC (Dynamic Range control) in DAC path.
- The high-pass filter in ADC path.
- Soft pop noise suppression.

- SAR-ADC(Successive Approximation Register)
  - 8-channel single-ended 10-bit SAR analog-to-digital converter
  - Sample rate Fs is 200KHz

## 1.3 Block Diagram

The following diagram shows the basic block diagram.

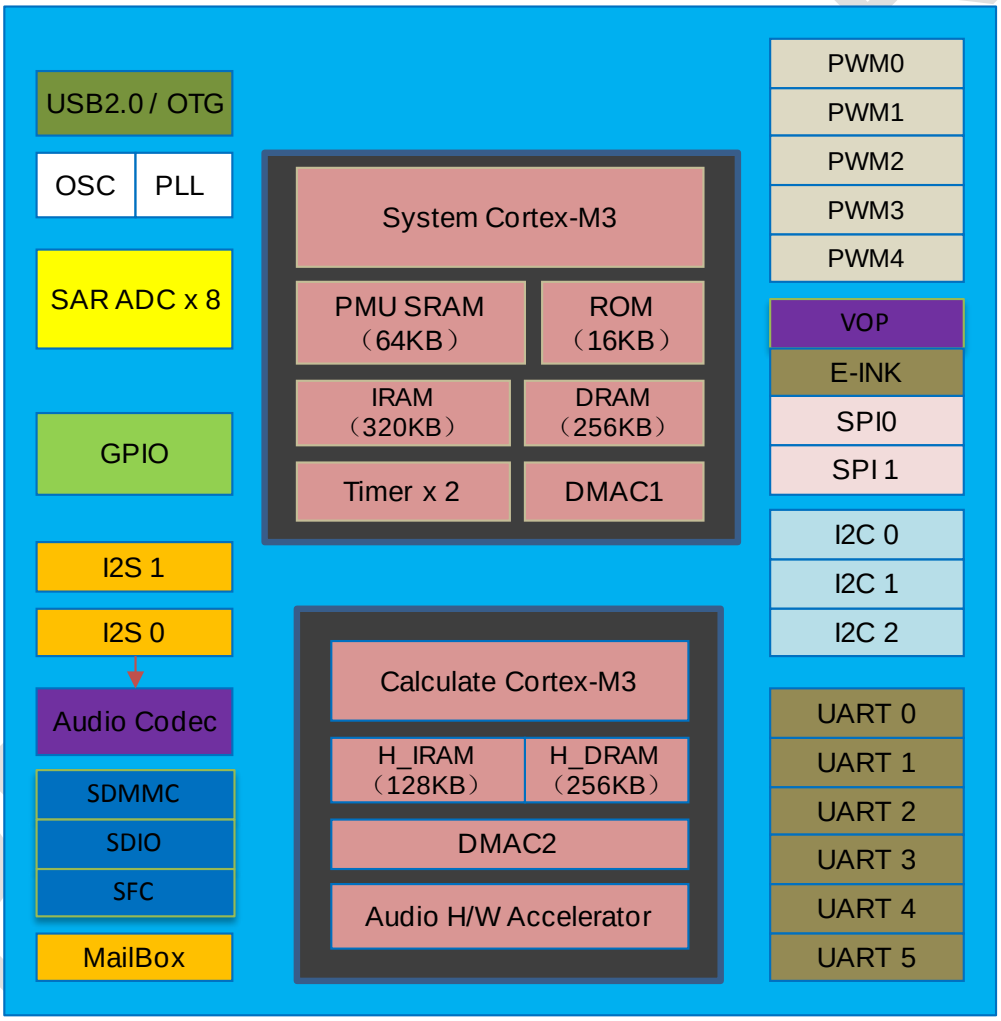


Fig.1-1Block Diagram

# Chapter 2 Package information

## 2.1 Ordering information

| Orderable Device | RoHS status | Package | Package Qty | Device special feature |
|---|---|---|---|---|
| RKNanoD-N | Pb-Free | QFN68 | | Embed M3 controller SOC |
| RKNanoD-G | Pb-Free | LFBGA121 | | Embed M3 controller SOC |

## 2.2 Dimension

### 2.2.1 QFN68 Package

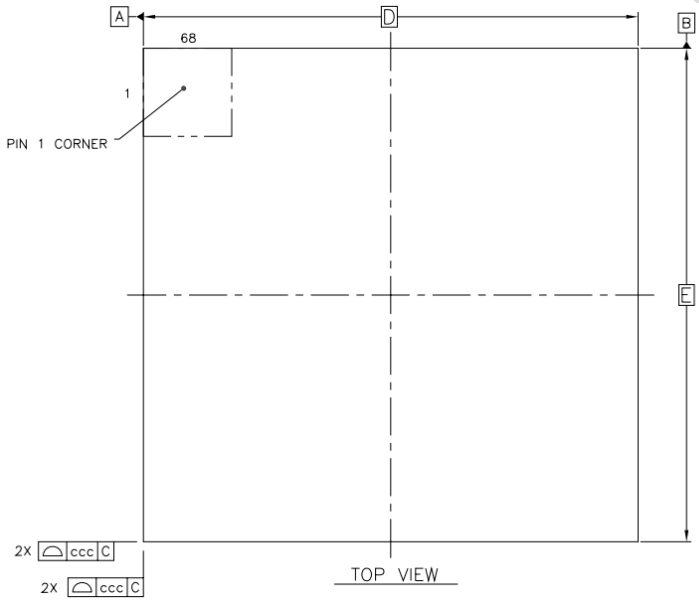


Fig. 2-1 RKNanoD-N QFN68 Package Top View

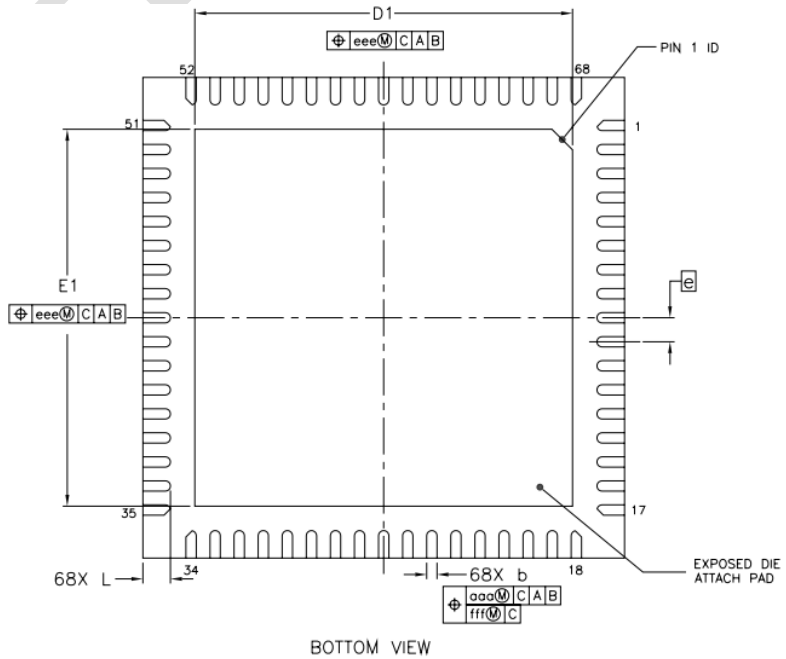


Fig. 2-2 RKNanoD-N QFN68 Package Bottom View

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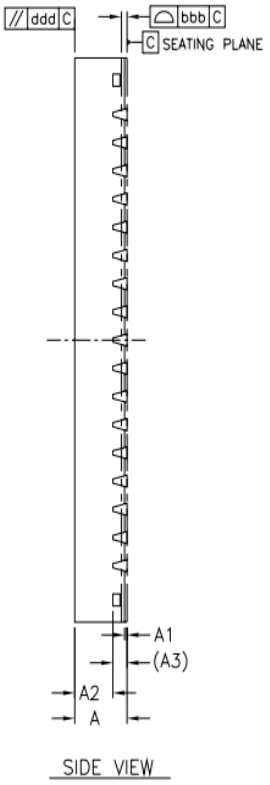


Fig. 2-3 RKNanoD-N QFN68 Package Side View

| FOR CUSTOMER ONLY | | | | |
|---|---|---|---|---|
| PACKAGE TYPE | QFN | | | |
| PIN COUNT | 68 | | | |
| DESCRIPTION | SYMBOL | MILLIMETER | | |
| | | MIN | NOM | MAX |
| TOTAL THICKNESS | A | 0.70 | 0.75 | 0.80 |
| STAND OFF | A1 | 0 | 0.035 | 0.05 |
| MOLD THICKNESS | A2 | – | 0.55 | 0.57 |
| MATERIAL THICKNESS | A3 | – | 0.203 REF | – |
| PACKAGE SIZE | D | – | 7 BSC | – |
| | E | – | 7 BSC | – |
| EP SIZE | D1 | 5.39 | 5.49 | 5.59 |
| | E1 | 5.39 | 5.49 | 5.59 |
| LEAD LENGTH | L | 0.30 | 0.40 | 0.50 |
| LEAD PITCH | e | 0.35 BSC | | |
| LEAD WIDTH | b | 0.10 | 0.15 | 0.20 |
| LEAD POSITION OFFSET | aaa | 0.07 | | |
| LEAD COPLANARITY | bbb | 0.08 | | |
| PACKAGE EDGE PROFILE | ccc | 0.10 | | |
| MOLD FLATNESS | ddd | 0.10 | | |
| EP POSITION OFFSET | eee | 0.10 | | |
| | fff | 0.05 | | |

Fig. 2-4 RKNanoD-N QFN68 Package Dimension

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### 2.2.2 LFBGA121 Package

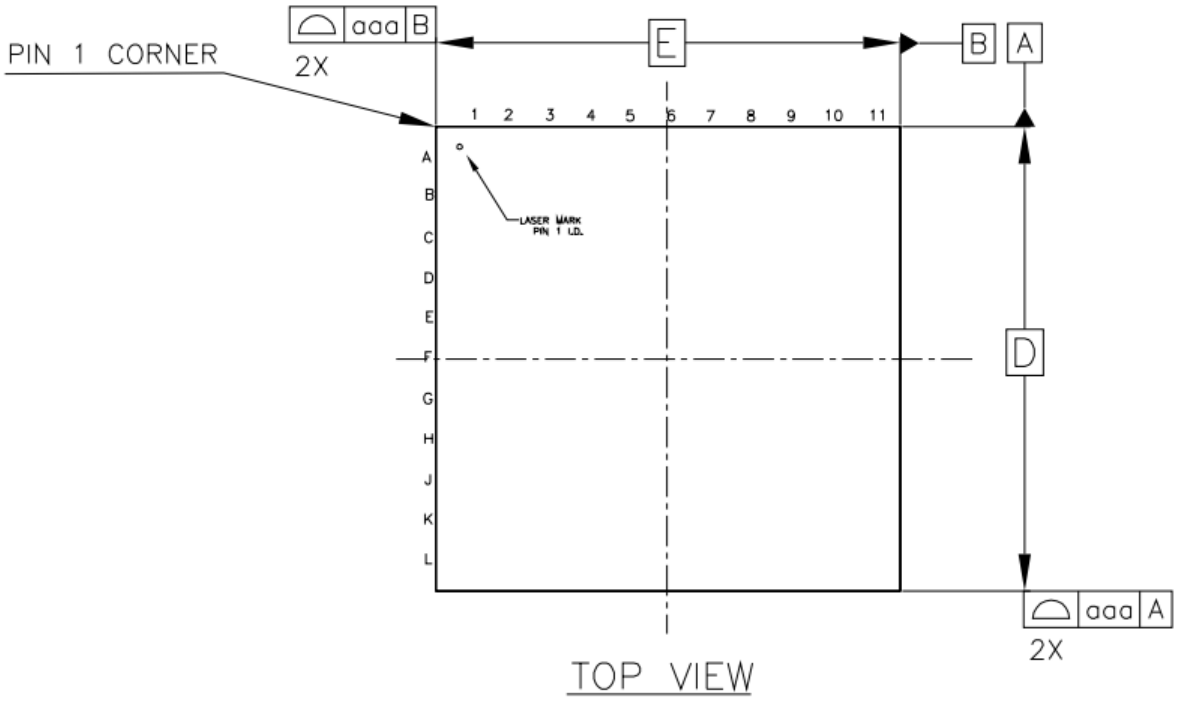


Fig. 2-5 RKNanoD-G LFBGA121 Package Top View

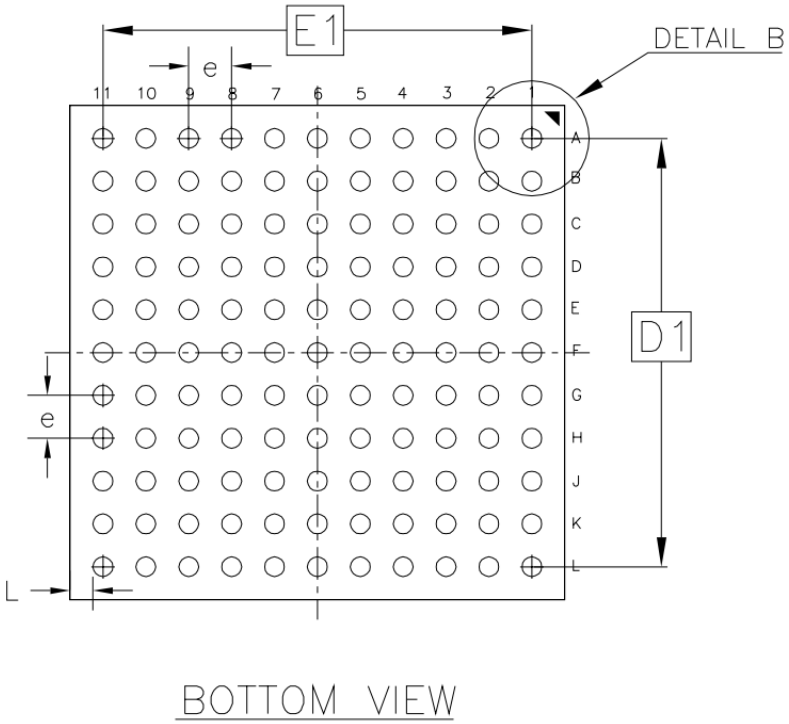


Fig. 2-6 RKNanoD-G LFBGA121 Package BOTTOM View

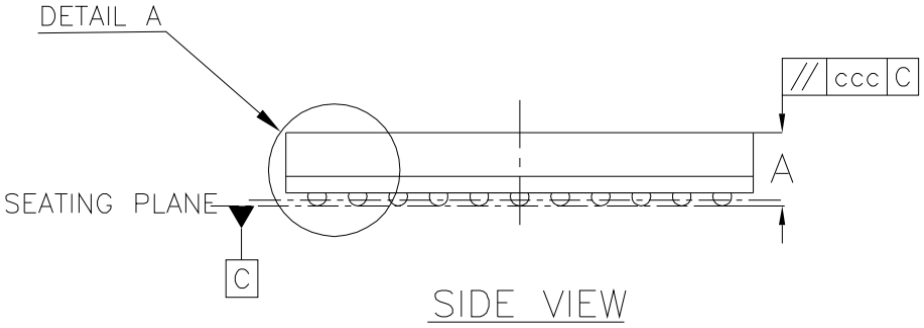


Fig. 2-7 RKNanoD-G LFBGA121 Package SIDE View

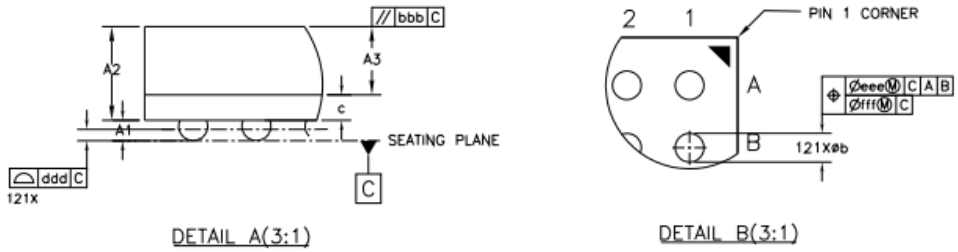


Fig. 2-8 RKNanoD-G LFBGA121 Package DETAIL A & B

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | -- | 1.25 |
| A1 | 0.16 | 0.21 | 0.26 |
| A2 | 0.91 | 0.96 | 1.01 |
| A3 | 0.70 BASIC | | |
| c | 0.21 | 0.26 | 0.31 |
| D | 7.40 | 7.50 | 7.60 |
| D1 | 6.50 BASIC | | |
| E | 7.40 | 7.50 | 7.60 |
| E1 | 6.50 BASIC | | |
| e | 0.65 BASIC | | |
| L | 0.35 REF | | |
| b | 0.25 | 0.30 | 0.35 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.20 | | |
| ddd | 0.08 | | |
| eee | 0.15 | | |
| fff | 0.08 | | |

Fig. 2-9 RKNanoD-G LFBGA121 Package Dimension

## 2.3 RKNanoD PIN Description

### 2.3.1 RKNanoD-N PIN Description

Table 2-1 RKNanoD-N Pin Information

| PIN | PIN_Name | Fountion0 | Fountion1 | Fountion2 | Fountion3 | Pull[®] | Pin types[®] | Power Domain[®] |
|---|---|---|---|---|---|---|---|---|
| 1 | I2C2C_SDA/JTG0_TRST/POWERHOLD/GPIOP2_A6 | GPIOP2_A6 | I2C2C_SDA | JTG0_TRST | POWERHOLD | down | I/O | IO |
| 2 | UART1A_RX/I2C0B_SCL/SPI1B_TX/GPIOP2_C1 | GPIOP2_C1 | UART1A_RX | I2C0B_SCL | SPI1B_TX | up | I/O | IO |
| 3 | UART1A_TX/I2C0B_SDA/SPI1B_CLK/GPIOP2_C0 | GPIOP2_C0 | UART1A_TX | I2C0B_SDA | SPI1B_CLK | up | I/O | IO |
| 4 | VDD | VDD | | | | | DP | |
| 5 | XOUT24M | XOUT24M | | | | | O | IO |
| 6 | XIN24M | XIN24M | | | | | I | IO |
| 7 | VDD_PLL | VDD_PLL | | | | | AP | PLL |
| 8 | VCC_PLL | VCC_PLL | | | | | AP | PLL |
| 9 | VCC | VCC | | | | | DP | IO |
| 10 | SDMMC_CMD/SPI1A_CS/UART3_TX/GPIO1_A5 | GPIO1_A5 | SDMMC_CMD | SPI1A_CS | UART3_TX | up | I/O | IO |
| 11 | SDMMC_CLK/SPI1A_CLK/UART3_RX/GPIO1_A6 | GPIO1_A6 | SDMMC_CLK | SPI1A_CLK | UART3_RX | up | I/O | IO |
| 12 | SDMMC_D0/SPI1A_RX/UART4_TX/GPIO1_A7 | GPIO1_A7 | SDMMC_D0 | SPI1A_RX | UART4_TX | up | I/O | IO |
| 13 | SDMMC_D1/SPI1A_TX/UART4_RX/GPIO1_B0 | GPIO1_B0 | SDMMC_D1 | SPI1A_TX | UART4_RX | up | I/O | IO |
| 14 | SDMMC_D2/I2C1B_SCL/UART5_TX/GPIO1_B1 | GPIO1_B1 | SDMMC_D2 | I2C1B_SCL | UART5_TX | up | I/O | IO |
| 15 | SDMMC_D3/I2C1B_SDA/UART5_RX/GPIO1_B2 | GPIO1_B2 | SDMMC_D3 | I2C1B_SDA | UART5_RX | up | I/O | IO |
| 16 | VDD | VDD | | | | | DP | |
| 17 | USB_DM | USB_DM | UART0B_RX | | | | A | USB |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 18 | USB_DP | USB_DP | UART0B_TX | | | | A | USB |
| 19 | VBUS | VBUS | | | | | I | USB |
| 20 | USB_VDD12 | USB_VDD12 | | | | | DP | USB |
| 21 | USB_EXTR | USB_EXTR | | | | | I | USB |
| 22 | AVDD_IO/USB_VCC33 | AVDD_IO | USB_VCC33 | | | | AP | USB |
| 23 | AVSS_IO | AVSS_IO | | | | | AG | USB |
| 24 | HPL_OUT | HPL_OUT | | | | | A | USB |
| 25 | HP_SENSE | HP_SENSE | | | | | A | USB |
| 26 | HP_VGND | HP_VGND | | | | | A | USB |
| 27 | HPR_OUT | HPR_OUT | | | | | A | USB |
| 28 | VREF | VREF | | | | | A | USB |
| 29 | MICBIAS_L | MICBIAS_L | | | | | A | USB |
| 30 | MIC1N | MIC1N | | | | | A | USB |
| 31 | MIC1P | MIC1P | | | | | A | USB |
| 32 | IN1R | IN1R | MIC2N | | | | A | USB |
| 33 | IN1L | IN1L | MIC2P | | | | A | USB |
| 34 | AVSS | AVSS | | | | | AG | ACODEC |
| 35 | AVDD | AVDD | | | | | AP | ACODEC |
| 36 | ADC0 | ADC0 | | | | | A | IO |
| 37 | ADC1 | ADC1 | | | | | A | IO |
| 38 | VCC/ADC_VCC33 | VCC | ADC_VCC33 | | | | DP | IO |
| 39 | EMMC_PWREN/I2S1B_CLK/GPIO0_A0 | GPIO0_A0 | EMMC_PWREN | I2S1B_CLK | | down | I/O | IO |
| 40 | EMMC_CLK/I2S1B_LRCK/UART2C_TX/GPIO0A1 | GPIO0A1 | EMMC_CLK | I2S1B_LRCK | UART2C_TX | down | I/O | IO |
| 41 | EMMC_CMD/I2S1B_SCLK/UART2C_RX/GPIO0_A2 | GPIO0_A2 | EMMC_CMD | I2S1B_SCLK | UART2C_RX | up | I/O | IO |
| 42 | EMMC_D0/I2S1B_SDO/UART2C_CTS/GPIO0_A3 | GPIO0_A3 | EMMC_D0 | I2S1B_SDO | UART2C_CTS | up | I/O | IO |
| 43 | EMMC_D1/I2S1B_SDI/UART2C_RTS/GPIO0_A4 | GPIO0_A4 | EMMC_D1 | I2S1B_SDI | UART2C_RTS | up | I/O | IO |
| 44 | EMMC_D2/SFC_D3/I2C0C_SDA/GPIO0_A5 | GPIO0_A5 | EMMC_D2 | SFC_D3 | I2C0C_SDA | up | I/O | IO |
| 45 | EMMC_D3/SFC_D2/I2C0C_SCL/GPIO0_A6 | GPIO0_A6 | EMMC_D3 | SFC_D2 | I2C0C_SCL | up | I/O | IO |
| 46 | EMMC_D4/SFC_D1/GPIO0_A7 | GPIO0_A7 | EMMC_D4 | SFC_D1 | | up | I/O | IO |
| 47 | EMMC_D5/SFC_D0/JTG1_TDI/GPIO0_B0 | GPIO0_B0 | EMMC_D5 | SFC_D0 | JTG1_TDI | up | I/O | IO |
| 48 | EMMC_D6/SFC_CLK/JTG1_TDO/GPIO0_B1 | GPIO0_B1 | EMMC_D6 | SFC_CLK | JTG1_TDO | up | I/O | IO |
| 49 | EMMC_D7/SFC_CS/JTG1_TRST/GPIO0_B2 | GPIO0_B2 | EMMC_D7 | SFC_CS | JTG1_TRST | up | I/O | IO |
| 50 | VDD | VDD | | | | | DP | |
| 51 | LCD_D0/SPI0A_TX/GPIO0_C0 | GPIO0_C0 | LCD_D0 | SPI0A_TX | | up | I/O | IO |
| 52 | LCD_D1/SPI0A_RX/GPIO0_C1 | GPIO0_C1 | LCD_D1 | SPI0A_RX | | up | I/O | IO |
| 53 | LCD_D2/SPI0A_CLK/GPIO0_C2 | GPIO0_C2 | LCD_D2 | SPI0A_CLK | | up | I/O | IO |
| 54 | LCD_D3/SPI0A_CS/GPIO0_C3 | GPIO0_C3 | LCD_D3 | SPI0A_CS | | up | I/O | IO |
| 55 | LCD_D4/UART2B_RX/GPIO0_C4 | GPIO0_C4 | LCD_D4 | UART2B_RX | | up | I/O | IO |
| 56 | LCD_D5/UART2B_TX/GPIO0_C5 | GPIO0_C5 | LCD_D5 | UART2B_TX | | up | I/O | IO |
| 57 | LCD_D6/UART2B_RTS/GPIO0_C6 | GPIO0_C6 | LCD_D6 | UART2B_RTS | | up | I/O | IO |
| 58 | LCD_D7/UART2B_CTS/GPIO0_C7 | GPIO0_C7 | LCD_D7 | UART2B_CTS | | up | I/O | IO |
| 59 | LCD_WRN/I2C2B_SCL/GPIO0_D0 | GPIO0_D0 | LCD_WRN | I2C2B_SCL | | up | I/O | IO |
| 60 | LCD_RS/I2C2B_SDA/GPIO0_D1 | GPIO0_D1 | LCD_RS | I2C2B_SDA | | up | I/O | IO |
| 61 | VDD | VDD | | | | | DP | |
| 62 | VCC | VCC | | | | | DP | IO |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 63 | UART1A_RTS/JTG0_TMS/SPI1B_CS/GPIOP2_B6 | GPIOP2_B6 | UART1A_RTS | JTG0_TMS | SPI1B_CS | up | I/O | IO |
| 64 | UART1A_CTS/JTG0_TCK/SPI1B_RX/GPIOP2_B7 | GPIOP2_B7 | UART1A_CTS | JTG0_TCK | SPI1B_RX | up | I/O | IO |
| 65 | RESET | RESET | | | | | I | IO |
| 66 | PWM1/CLK_OBS/EBC_GDPWR1/GPIOP2_A3 | GPIOP2_A3 | PWM1 | CLK_OBS | | | I/O | IO |
| 67 | PWM0/JTG0_TDI/PMU_ST2/GPIOP2_A4 | GPIOP2_A4 | PWM0 | JTG0_TDI | PMU_ST2 | | I/O | IO |
| 68 | I2C2C_SCL/JTG0_TDO/PMU_ST1/GPIOP2_A5 | GPIOP2_A5 | I2C2C_SCL | JTG0_TDO | PLAYON | down | I/O | IO |
| 69 | GND | | | | | | DG | |

Note:

①:Pin types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②:The pull up/pull down can be disabled.

③: **POWERHOLD and PLAYON are defined by software.**

④: Power domain
IO: power supply for system and logic
PLL: power supply for PLL
USB: power supply for USB and ACODEC IO
ACODEC: power supply for ACODEC core

### 2.3.2 RKNanoD-G ball Description

Table 2-2 RKNanoD-G ball information

| Ball | Ball_Name | Fountion0 | Fountion1 | Fountion2 | Fountion3 | Pull② | Pinty pes① | Power Domain④ |
|---|---|---|---|---|---|---|---|---|
| A1 | I2C2C_SDA/JTG0_TRST/POWERHOLD/GPIOP2_A6 | GPIOP2_A6 | I2C2C_SDA | JTG0_TRST | POWERHOLD | down | I/O | PMU |
| A2 | I2C2C_SCL/JTG0_TDO/PLAYON/GPIOP2_A5 | GPIOP2_A5 | I2C2C_SCL | JTG0_TDO | PLAYON | down | I/O | PMU |
| A3 | PWM0/JTG0_TDI/PMU_ST2/GPIOP2_A4 | GPIOP2_A4 | PWM0 | JTG0_TDI | PMU_ST2 | down | I/O | PMU |
| A4 | UART1A_CTS/JTG0_TCK/SPI1B_RX/GPIOP2_B7 | GPIOP2_B7 | UART1A_CTS | JTG0_TCK | SPI1B_RX | up | I/O | PMU |
| A5 | PWM3/I2C2A_SCL/EBC_SDCE0/GPIOP2_A1 | GPIOP2_A1 | PWM3 | I2C2A_SCL | EBC_SDCE0 | up | I/O | PMU |
| A6 | I2C1A_SDA/SPI0B_CS/EBC_SDCE3/GPIOP2_B0 | GPIOP2_B0 | I2C1A_SDA | SPI0B_CS | EBC_SDCE3 | up | I/O | PMU |
| A7 | UART2A_TX/I2S0_LRCK/EBC_GDSP/GPIO0_B6 | GPIO0_B6 | UART2A_TX | I2S0_LRCK | EBC_GDSP | up | I/O | IO1 |
| A8 | LCD_D7/UART2B_CTS/EBC_SDDO7/GPIO0_C7 | GPIO0_C7 | LCD_D7 | UART2B_CTS | EBC_SDDO7 | up | I/O | IO1 |
| A9 | LCD_D4/UART2B_RX/EBC_SDDO4/GPIO0_C4 | GPIO0_C4 | LCD_D4 | UART2B_RX | EBC_SDDO4 | up | I/O | IO1 |
| A10 | LCD_D1/SPI0A_RX/EBC_SDDO1/GPIO0_C1 | GPIO0_C1 | LCD_D1 | SPI0A_RX | EBC_SDDO1 | up | I/O | IO1 |
| A11 | LCD_D0/SPI0A_TX/EBC_SDDO0/GPIO0_C0 | GPIO0_C0 | LCD_D0 | SPI0A_TX | EBC_SDDO0 | up | I/O | IO1 |
| B1 | PWM1/CLK_OBS/EBC_GDPWR1/GPIOP2_A3 | GPIOP2_A3 | PWM1 | CLK_OBS | EBC_GDPWR1 | up | I/O | PMU |
| B2 | RESET | RESET | | | | down | I | PMU |
| B3 | UART1A_RTS/JTG0_TMS/SPI1B_CS/GPIOP2_B6 | GPIOP2_B6 | UART1A_RTS | JTG0_TMS | SPI1B_CS | up | I/O | PMU |
| B4 | PWM2/EBC_GDPWR2/PMU_ST3/GPIOP2_A2 | GPIOP2_A2 | PWM2 | EBC_GDPWR2 | PMU_ST3 | down | I/O | PMU |
| B5 | PWM4/I2C2A_SDA/EBC_GDPWR0/GPIOP2_A0 | GPIOP2_A0 | PWM4 | I2C2A_SDA | EBC_GDPWR0 | up | I/O | PMU |
| B6 | UART2A_RTS/I2S0_SDI/EBC_VCOM/GPIO0_B3 | GPIO0_B3 | UART2A_RTS | I2S0_SDI | EBC_VCOM | up | I/O | IO1 |
| B7 | UART2A_RX/I2S0_SCLK/EBC_GDCLK/GPIO0_B5 | GPIO0_B5 | UART2A_RX | I2S0_SCLK | EBC_GDCLK | up | I/O | IO1 |
| B8 | LCD_CSN/I2S0_CLK/EBC_GDOE/GPIO0_B7 | GPIO0_B7 | LCD_CSN | I2S0_CLK | EBC_GDOE | up | I/O | IO1 |
| B9 | LCD_WRN/I2C2B_SCL/EBC_SDLE/GPIO0_D0 | GPIO0_D0 | LCD_WRN | I2C2B_SCL | EBC_SDLE | up | I/O | IO1 |
| B10 | LCD_D5/UART2B_TX/EBC_SDDO5/GPIO0_C5 | GPIO0_C5 | LCD_D5 | UART2B_TX | EBC_SDDO5 | up | I/O | IO1 |
| B11 | LCD_D2/SPI0A_CLK/EBC_SDDO2/GPIO0_C2 | GPIO0_C2 | LCD_D2 | SPI0A_CLK | EBC_SDDO2 | up | I/O | IO1 |
| C1 | UART0A_TX/JTG1_TCK/I2C1C_SCL/GPIOP2_B5 | GPIOP2_B5 | UART0A_TX | JTG1_TCK | I2C1C_SCL | up | I/O | PMU |
| C2 | UART0A_RX/JTG1_TMS/I2C1C_SDA/GPIOP2_B4 | GPIOP2_B4 | UART0A_RX | JTG1_TMS | I2C1C_SDA | up | I/O | PMU |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| C3 | PMU_IDLE/GPIOP2_A7 | GPIOP2_A7 | PMU_IDLE | | | down | I/O | PMU |
| C4 | VCC_PMU | VCC_PMU | | | | | DP | PMU |
| C5 | I2C1A_SCL/SPI0B_CLK/EBC_BORDER1/GPIOP2_B1 | GPIOP2_B1 | I2C1A_SCL | SPI0B_CLK | EBC_BORDER1 | up | I/O | PMU |
| C6 | UART2A_CTS/I2S0_SDO/EBC_SDCLK/GPIO0_B4 | GPIO0_B4 | UART2A_CTS | I2S0_SDO | EBC_SDCLK | up | I/O | IO1 |
| C7 | VDD | VDD | | | | | DP | |
| C8 | LCD_RS/I2C2B_SDA/EBC_SDOE/GPIO0_D1 | GPIO0_D1 | LCD_RS | I2C2B_SDA | EBC_SDOE | up | I/O | IO1 |
| C9 | LCD_D6/UART2B_RTS/EBC_SDDO6/GPIO0_C6 | GPIO0_C6 | LCD_D6 | UART2B_RTS | EBC_SDDO6 | up | I/O | IO1 |
| C10 | EMMC_D4/SFC_D1/GPIO0_A7 | GPIO0_A7 | EMMC_D4 | SFC_D1 | | up | I/O | IO0 |
| C11 | LCD_D3/SPI0A_CS/EBC_SDDO3/GPIO0_C3 | GPIO0_C3 | LCD_D3 | SPI0A_CS | EBC_SDDO3 | up | I/O | IO1 |
| D1 | XIN24M | XIN24M | | | | | I | PMU |
| D2 | UART1A_TX/I2C0B_SDA/SPI1B_CLK/GPIOP2_C0 | GPIOP2_C0 | UART1A_TX | I2C0B_SDA | SPI1B_CLK | up | I/O | PMU |
| D3 | UART1A_RX/I2C0B_SCL/SPI1B_TX/GPIOP2_C1 | GPIOP2_C1 | UART1A_RX | I2C0B_SCL | SPI1B_TX | up | I/O | PMU |
| D4 | VDD_PMU | VDD_PMU | | | | | DP | PMU |
| D5 | I2C0A_SCL/SPI0B_TX/EBC_SDCE5/GPIOP2_B2 | GPIOP2_B2 | I2C0A_SCL | SPI0B_TX | EBC_SDCE5 | up | I/O | PMU |
| D6 | VSS | VSS | | | | | DG | PMU |
| D7 | VCC_1 | VCC_1 | | | | | DP | IO1 |
| D8 | VSS | VSS | | | | | DG | |
| D9 | EMMC_D2/SFC_D3/I2C0C_SDA/GPIO0_A5 | GPIO0_A5 | EMMC_D2 | SFC_D3 | I2C0C_SDA | up | I/O | IO0 |
| D10 | EMMC_D5/SFC_D0/JTG1_TDI/GPIO0_B0 | GPIO0_B0 | EMMC_D5 | SFC_D0 | JTG1_TDI | up | I/O | IO0 |
| D11 | EMMC_D6/SFC_CLK/JTG1_TDO/GPIO0_B1 | GPIO0_B1 | EMMC_D6 | SFC_CLK | JTG1_TDO | up | I/O | IO0 |
| E1 | VDD_PLL | VDD_PLL | | | | | AP | PLL |
| E2 | XOUT24M | XOUT24M | | | | | I | PMU |
| E3 | PMU_TEST | PMU_TEST | | | | | I | PMU |
| E4 | SDMMC_CMD/SPI1A_CS/UART3_TX/GPIO1_A5 | GPIO1_A5 | SDMMC_CMD | SPI1A_CS | UART3_TX | up | I/O | IO2 |
| E5 | I2C0A_SDA/SPI0B_RX/EBC_BORDER0/GPIOP2_B3 | GPIOP2_B3 | I2C0A_SDA | SPI0B_RX | EBC_BORDER0 | up | I/O | PMU |
| E6 | VSS | VSS | | | | | DG | |
| E7 | VSS | VSS | | | | | DG | |
| E8 | VSS | VSS | | | | | DG | |
| E9 | VCC_0 | VCC_0 | | | | | DP | IO0 |
| E10 | EMMC_D3/SFC_D2/I2C0C_SCL/GPIO0_A6 | GPIO0_A6 | EMMC_D3 | SFC_D2 | I2C0C_SCL | up | I/O | IO0 |
| E11 | EMMC_D7/SFC_CS/JTG1_TRST/GPIO0_B2 | GPIO0_B2 | EMMC_D7 | SFC_CS | JTG1_TRST | up | I/O | IO0 |
| F1 | VCC_PLL | VCC_PLL | | | | | DP | PLL |
| F2 | SDMMC_D1/SPI1A_TX/UART4_RX/GPIO1_B0 | GPIO1_B0 | SDMMC_D1 | SPI1A_TX | UART4_RX | up | I/O | IO2 |
| F3 | SDMMC_D2/I2C1B_SCL/UART5_TX/GPIO1_B1 | GPIO1_B1 | SDMMC_D2 | I2C1B_SCL | UART5_TX | up | I/O | IO2 |
| F4 | SDMMC_CLK/SPI1A_CLK/UART3_RX/GPIO1_A6 | GPIO1_A6 | SDMMC_CLK | SPI1A_CLK | UART3_RX | up | I/O | IO2 |
| F5 | ADC5 | ADC5 | | | | | A | ADC |
| F6 | ADC4 | ADC4 | | | | | A | ADC |
| F7 | VSS | VSS | | | | | DG | |
| F8 | VDD | VDD | | | | | DP | |
| F9 | VCC_0 | VCC_0 | | | | | DP | IO0 |
| F10 | EMMC_D0/I2S1B_SDO/UART2C_CTS/GPIO0_A3 | GPIO0_A3 | EMMC_D0 | I2S1B_SDO | UART2C_CTS | up | I/O | IO0 |
| F11 | EMMC_D1/I2S1B_SDI/UART2C_RTS/GPIO0_A4 | GPIO0_A4 | EMMC_D1 | I2S1B_SDI | UART2C_RTS | up | I/O | IO0 |
| G1 | I2S1A_CLK/EBC_GDRL/GPIO1_A0 | GPIO1_A0 | I2S1A_CLK | EBC_GDRL | | down | I/O | IO2 |
| G2 | SDMMC_D3/I2C1B_SDA/UART5_RX/GPIO1_B2 | GPIO1_B2 | SDMMC_D3 | I2C1B_SDA | UART5_RX | up | I/O | IO2 |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| G3 | SDMMC_D0/SPI1A_RX/UART4_TX/GPIO1_A7 | GPIO1_A7 | SDMMC_D0 | SPI1A_RX | UART4_TX | up | I/O | IO2 |
| G4 | VCC_2 | VCC_2 | | | | | DP | IO2 |
| G5 | ADC3 | ADC3 | | | | | A | ADC |
| G6 | ADC6 | ADC6 | | | | | A | ADC |
| G7 | ADC7 | ADC7 | | | | | A | ADC |
| G8 | ADC_VSS | ADC_VSS | | | | | AG | ADC |
| G9 | ADC_REF_OUT | ADC_REF_OUT | | | | | A | ADC |
| G10 | EMMC_CMD/I2S1B_SCLK/UART2C_RX/GPIO0_A2 | GPIO0_A2 | EMMC_CMD | I2S1B_SCLK | UART2C_RX | up | I/O | IO0 |
| G11 | EMMC_CLK/I2S1B_LRCK/UART2C_TX/GPIO0_A1 | GPIO0_A1 | EMMC_CLK | I2S1B_LRCK | UART2C_TX | down | I/O | IO0 |
| H1 | I2S1A_SCLK/UART1B_TX/EBC_SDCE2/GPIO1_A2 | GPIO1_A2 | I2S1A_SCLK | UART1B_TX | EBC_SDCE2 | down | I/O | IO2 |
| H2 | IO_TEST | IO_TEST | | | | | I | IO2 |
| H3 | VDD | VDD | | | | | DG | |
| H4 | VCC_2 | VCC_2 | | | | | DP | IO2 |
| H5 | ADC1 | ADC1 | | | | | A | ADC |
| H6 | ADC0 | ADC0 | | | | | A | ADC |
| H7 | ADC2 | ADC2 | | | | | A | ADC |
| H8 | ADC_VCC33 | ADC_VCC33 | | | | | AP | ADC |
| H9 | ADC_VREF | ADC_VREF | | | | | A | ADC |
| H10 | EMMC_PWREN/I2S1B_CLK/GPIO0_A0 | GPIO0_A0 | EMMC_PWREN | I2S1B_CLK | | down | I/O | IO0 |
| H11 | EMMC_RSTN/GPIO1_B3 | GPIO1_B3 | EMMC_RSTN | | | down | I/O | IO0 |
| J1 | I2S1A_SDI/UART1B_RTS/EBC_SDCE4/GPIO1_A4 | GPIO1_A4 | I2S1A_SDI | UART1B_RTS | EBC_SDCE4 | down | I/O | IO2 |
| J2 | I2S1A_SDO/UART1B_CTS/EBC_SDCE1/GPIO1_A3 | GPIO1_A3 | I2S1A_SDO | UART1B_CTS | EBC_SDCE1 | down | I/O | IO2 |
| J3 | I2S1A_LRCK/UART1B_RX/EBC_SDSHR/GPIO1_A1 | GPIO1_A1 | I2S1A_LRCK | UART1B_RX | EBC_SDSHR | down | I/O | IO2 |
| J4 | VSS | VSS | | | | | DG | |
| J5 | USB_VSSA | USB_VSSA | | | | | AG | USB |
| J6 | MICBIAS_R | MICBIAS_R | | | | | A | USB |
| J7 | MICBIAS_L | MICBIAS_L | | | | | A | USB |
| J8 | AVSS | AVSS | | | | | AG | ACODEC |
| J9 | AVDD | AVDD | | | | | AP | ACODEC |
| J10 | IN2L | IN2L | | | | | A | USB |
| J11 | IN1R | IN1R | | | | | A | USB |
| K1 | USB_EXTR | USB_EXTR | | | | | A | USB |
| K2 | AVSS_IO | AVSS_IO | | | | | AG | USB |
| K3 | VDD | VDD | | | | | DP | IO |
| K4 | VBUS | VBUS | | | | | I | USB |
| K5 | AVDD_IO/USB_VCC33 | AVDD_IO | USB_VCC33 | | | | AP | USB |
| K6 | HPR_OUT | HPR_OUT | | | | | A | USB |
| K7 | HP_SENSE | HP_SENSE | | | | | A | USB |
| K8 | MIC1P | MIC1P | | | | | A | USB |
| K9 | MIC2P | MIC2P | | | | | A | USB |
| K10 | IN2R | IN2R | | | | | A | USB |
| K11 | IN1L | IN1L | | | | | A | USB |
| L1 | USB_DM | USB_DM | UART0B_RX | | | | A | USB |
| L2 | USB_DP | USB_DP | UART0B_TX | | | | A | USB |
| L3 | USB_VDD12 | USB_VDD12 | | | | | AP | USB |

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| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| L4 | USB_ID | USB_ID | | | | | I | USB |
| L5 | HPL_OUT | HPL_OUT | | | | | A | USB |
| L6 | HP_VGND | HP_VGND | | | | | A | USB |
| L7 | MIC1N | MIC1N | | | | | A | USB |
| L8 | MIC2N | MIC2N | | | | | A | USB |
| L9 | LINEOUT_R | LINEOUT_R | | | | | A | USB |
| L10 | LINEOUT_L | LINEOUT_L | | | | | A | USB |
| L11 | VREF | VREF | | | | | A | USB |

Note:

①:Pin types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②:The pull up/pull down can be disabled.

③: Power domain
PMU: power supply for PMU(always on logic), the GPIOs of this power domain can wake up system
from sleep mode
PLL: power supply for PLL
USB: power supply for USB and ACODEC IO
ACODEC: power supply for ACODEC core
ADC: power supply for ADC
IO0: power supply from VCC_0
IO1: power supply from VCC_1
IO2: power supply from VCC_2

Table 2-3 RKNanoD-G ball map

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | POWERHOLD | PLAYON | PWM0 | UART1A_CTS | PWM3 | I2C1A_SDA | UART2A_TX | LCD_D7 | LCD_D4 | LCD_D1 | LCD_D0 |
| B | PWM1 | RESET | UART1A_RTS | PWM2 | PWM4 | UART2A_RTS | UART2A_RX | LCD_CSN | LCD_WRN | LCD_D5 | LCD_D2 |
| C | UART0A_TX | UART0A_RX | PMU_IDLE | VCC_PMU0 | I2C1A_SCL | UART2A_CTS | VDD | LCD_RS | LCD_D6 | EMMC_D4 | LCD_D3 |
| D | XIN24M | UART1A_TX | UART1A_RX | VDD_PMU | I2C0A_SCL | VSS | VCC_1 | VSS | EMMC_D2 | EMMC_D5 | EMMC_D6 |
| E | VDD_PLL | XOUT24M | PMUTEST | SDMMC_CMD | I2C0A_SDA | VSS | VSS | VSS | VCC_0 | EMMC_D3 | EMMC_D7 |
| F | VCC_PLL | SDMMC_D1 | SDMMC_D2 | SDMMC_CLK | ADC5 | ADC4 | VSS | VDD | VCC_0 | EMMC_D0 | EMMC_D1 |
| G | I2S1A_CLK | SDMMC_D3 | SDMMC_D0 | VCC_2 | ADC3 | ADC6 | ADC7 | ADC_VSS | ADC_REF_OUT | EMMC_CMD | EMMC_CLK |
| H | I2S1A_SCLK | TEST_PAD | VDD | VCC_2 | ADC1 | ADC0 | ADC2 | ADC_VCC33 | ADC_VREF | EMMC_PWR_EN | EMMC_RSTN |

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| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **J** | I2S1A_SDI | I2S1A_SDO | I2S1A_LRCK | VSS | USB_VSSA | MICBIAS_R | MICBIAS_L | AVSS | AVDD | IN2L | IN1R |
| **K** | USB_EXTR | AVSS_IO | VDD | VBUS | AVDD_IO/USB_VCC33 | HPR_OUT | HP_SENSE | MIC1P | MIC2P | IN2R | IN1L |
| **L** | USB_DM | USB_DP | USB_VDD12 | USB_ID | HPL_OUT | HP_VGND | MIC1N | MIC2N | LINEOUT_R | LINEOUT_L | VREF |

## 2.4 RKNanoD Power/ground IO descriptions

Table 2-3 RKNanoD-N Power/Ground IO information

| Pin Name | Pin Number | Descriptions |
|---|---|---|
| VDD | 4,16,50,61 | Internal core Power |
| VCC | 9,38,62 | Digital IO Power Supply |
| VDD_PLL | 7 | PLL Analog Power Supply |
| VCC_PLL | 8 | PLL Analog Power Supply |
| USB_VDD12 | 20 | USB Analog Power Supply |
| AVDD_IO/USB_VCC33 | 22 | Codec and USB Analog Power Supply |
| AVSS_IO | 23 | Codec and USB Analog Ground |
| AVDD | 35 | Codec Analog Power Supply |
| AVSS | 34 | Codec and USB Analog Ground |
| GND | 69 | Digital Ground |

Table 2-4 RKNanoD-G Power/Ground IO information

| Ball Name | Ball Number | Descriptions |
|---|---|---|
| VDD | C7,F8,H3,K3 | Internal core Power |
| VCC_0 | E9,F9 | Digital IO Power Supply |
| VCC_1 | D7 | Digital IO Power Supply |
| VCC_2 | G4,H4 | Digital IO Power Supply |
| VDD_PMU | D4 | PMU Domain Logic Power Supply |
| VCC_PMU | C4 | PMU Domain IO Power Supply |
| VDD_PLL | E1 | PLL Analog Power Supply |
| VCC_PLL | F1 | PLL Analog Power Supply |
| ADC_VCC33 | H8 | SARADC Analog Power Supply |
| ADC_VSS | G8 | SARADC Analog Power Ground |
| AVDD | J9 | Codec Analog Power Supply |
| AVSS | J8 | Codec Analog Power Ground |
| USB_VDD12 | L3 | USB Analog Power Supply |
| USB_VSSA | J5 | USB Analog Ground |
| AVDD_IO/USB_VCC33 | K5 | Codec and USB Analog Power Supply |
| AVSS_IO | K2 | Codec and USB Analog Power Ground |
| VSS | D6,D8,E6,E7,E8,F7,J4 | Digital Power Ground |

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## 2.5 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-2 RKNanoD IO function description list

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| Misc | XIN24M | I | Clock input of 24MHz crystal |
| | XOUT24M | O | Clock output of 24MHz crystal |
| | RESET | I | Chip hardware reset |
| | CLK_OBS | O | Clock select output |
| | PMU_IDLE | O | PMU idle signal output |
| | PMU_TEST | I | Test pin |
| | IO_TEST | I | Test pin |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| JTAG0 | JTG0_TRST | I | JTAG0 interface reset input |
| | JTG0_TCK | I | JTAG0 interface clock input/SWD interface clock input |
| | JTG0_TDI | I | JTAG0 interface TDI input |
| | JTG0_TMS | I/O | JTAG0 interface TMS input/SWD interface data out |
| | JTG0_TDO | O | JTAG0 interface TDO output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| JTAG1 | JTG1_TRST | I | JTAG1 interface reset input |
| | JTG1_TCK | I | JTAG1 interface clock input/SWD interface clock input |
| | JTG1_TDI | I | JTAG1 interface TDI input |
| | JTG1_TMS | I/O | JTAG1 interface TMS input/SWD interface data out |
| | JTG1_TDO | O | JTAG1 interface TDO output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| eMMC Interface | EMMC_CLK | O | emmc flash clock. |
| | EMMC_CMD | I/O | emmc flash command output and reponse input. |
| | EMMC_D i (i=0~7) | I/O | emmc flash data input and output. |
| | EMMC_PWREN | O | emmc flash power-enable control signal |
| | EMMC_RSTN | O | emmc flash reset signal |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SDMMC Host Controller | SDMMC_CLK | O | sdmmc card clock. |
| | SDMMC_CMD | I/O | sdmmc card command output and reponse input. |
| | SDMMC_Di (i=0~3) | I/O | sdmmc card data input and output. |

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| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SFC Host Controller | SFC_CS | O | Serial flash chip select |
| | SFC_CLK | O | Serial flash clock output |
| | SFC_Di (i=0~3) | I/O | Serial flash data input/output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| LCDC | LCD_Di (i=0~7) | O | LCDC i8080 interface data output |
| | LCD_WRN | O | LCDC i8080 interface write enable |
| | LCD_RS | O | LCDC i8080 interface command/data signal |
| | LCD_CSN | O | LCDC i8080 interface chip select |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| EBC | EBC_SDCLK | O | Eink panel source clock |
| | EBC_SDLE | O | Eink panel source latch pulse |
| | EBC_SDOE | O | Eink panel source data output enable |
| | EBC_SDEC i (i=0~5) | O | Eink panel source data shift enable |
| | EBC_SDDO i (i=0~7) | O | Eink panel source data |
| | EBC_SDSHR | O | Eink panel source scan direction |
| | EBC_GDCLK | O | Eink panel gate clock |
| | EBC_GDOE | O | Eink panel gate output mode |
| | EBC_GDSP | O | Eink panel gate start pulse |
| | EBC_GDRL | O | Eink panel gate scan direction |
| | EBC_VCOM | O | Eink panel com voltage enable |
| | EBC_BORDER i (i=0,1) | O | Eink panel border output signal |
| | EBC_GDPWR i (i=0~2) | O | Eink panel power control signal |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SPI Interface | SPI0A_CLK | I/O | Spi0 port A serial clock |
| | SPI0A_CS | I/O | spi0 port A chip select signal, low active |
| | SPI0A_TX | O | spi0 port A serial data output |
| | SPI0A_RX | I | spi0 port A serial data input |
| | SPI0B_CLK | I/O | Spi0 port B serial clock |
| | SPI0B_CS | I/O | spi0 port B chip select signal, low active |
| | SPI0B_TX | O | spi0 port B serial data output |
| | SPI0B_RX | I | spi0 port B serial data input |
| | SPI1A_CLK | I/O | Spi1 port A serial clock |
| | SPI1A_CS | I/O | Spi1 port A chip select signal, low active |
| | SPI1A_TX | O | Spi1 port A serial data output |

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|---|---|---|---|
| | SPI1A_RX | I | Spi1 port A serial data input |
| | SPI1B_CLK | I/O | Spi1 port B serial clock |
| | SPI1B_CS | I/O | Spi1 port B chip select signal,low active |
| | SPI1B_TX | O | Spi1 port B serial data output |
| | SPI1B_RX | I | Spi1 port B serial data input |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| I2C master | I2C0A_SDA | I/O | I2C0 port A_ data |
| | I2C0A_SCL | O | I2C0 portA clock |
| | I2C0B_SDA | I/O | I2C0 port B_ data |
| | I2C0B_SCL | O | I2C0 portB clock |
| | I2C0C_SDA | I/O | I2C0 port C_ data |
| | I2C0C_SCL | O | I2C0 portC clock |
| | I2C1A_SDA | I/O | I2C1 port A_ data |
| | I2C1A_SCL | O | I2C1 portA clock |
| | I2C1B_SDA | I/O | I2C1 port B_ data |
| | I2C1B_SCL | O | I2C1 portB clock |
| | I2C1C_SDA | I/O | I2C1 port C_ data |
| | I2C1C_SCL | O | I2C1 portC clock |
| | I2C2A_SDA | I/O | I2C2 port A_ data |
| | I2C2A_SCL | O | I2C2portA clock |
| | I2C2B_SDA | I/O | I2C2 port B_ data |
| | I2C2B_SCL | O | I2C2 portB clock |
| | I2C2C_SDA | I/O | I2C2 port C_ data |
| | I2C2C_SCL | O | I2C2 portC clock |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| UART | UART0A_RX | I | UART0 port A serial data input |
| | UART0A_TX | O | UART0 port A serial data output |
| | UART0B_RX | I | UART0 port B serial data input |
| | UART0B_TX | O | UART0 port B serial data output |
| | UART1A_RX | I | UART1 port A serial data input |
| | UART1A_TX | O | UART1 port A serial data output |
| | UART1A_CTS | O | UART1 port A clear to send |
| | UART1A_RTS | I | UART1 port A request to send |
| | UART1B_RX | I | UART1 port B serial data input |
| | UART1B_TX | O | UART1 port B serial data output |
| | UART1B_CTS | O | UART1 port B clear to send |
| | UART1B_RTS | I | UART1 port B request to send |
| | UART2A_RX | I | UART2 port A serial data input |
| | UART2A_TX | O | UART2 port A serial data output |
| | UART2A_CTS | O | UART2 port A clear to send |
| | UART2A_RTS | I | UART2 port A request to send |
| | UART2B_RX | I | UART2 port B serial data input |
| | UART2B_TX | O | UART2 port B serial data output |
| | UART2B_CTS | O | UART2 port C clear to send |

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|---|---|---|---|
| | UART2B_RTS | I | UART2 port C request to send |
| | UART2C_RX | I | UART2 port C serial data input |
| | UART2C_TX | O | UART2 port C serial data output |
| | UART2C_CTS | O | UART2 port C clear to send |
| | UART2C_RTS | I | UART2 port C request to send |
| | UART3_RX | I | UART3 serial data input |
| | UART3_TX | O | UART3 serial data output |
| | UART4_RX | I | UART4 serial data input |
| | UART4_TX | O | UART4 serial data output |
| | UART5_RX | I | UART5 serial data input |
| | UART5_TX | O | UART5 serial data output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| I2S Controller | I2S0_CLK | O | I2S0 clock source |
| | I2S0_SCLK | I/O | I2S0 serial clock |
| | I2S0_LRCK | I/O | I2S0 left & right channel signal for serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S0_SDI | I | I2S0 serial data input |
| | I2S0_SDO | O | I2S0 serial data output |
| | I2S1A_CLK | O | I2S1 port A clock source |
| | I2S1A_SCLK | I/O | I2S1 port A serial clock |
| | I2S1A_LRCK | I/O | I2S1 port A left & right channel signal for serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S1A_SDI | I | I2S1 port A serial data input |
| | I2S1A_SDO | O | I2S1 port A serial data output |
| | I2S1B_CLK | O | I2S1 port B clock source |
| | I2S1B_SCLK | I/O | I2S1 port B serial clock |
| | I2S1B_LRCK | I/O | I2S1 port B left & right channel signal for serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S1B_SDI | I | I2S1 port B serial data input |
| | I2S1B_SDO | O | I2S1 port B serial data output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| PWM | PWM4 | O | Pulse Width Modulation output |
| | PWM3 | O | Pulse Width Modulation output |
| | PWM2 | O | Pulse Width Modulation output |
| | PWM1 | O | Pulse Width Modulation output |
| | PWM0 | O | Pulse Width Modulation output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SAR-ADC | ADC_REF_OUT | O | SAR-ADC reference voltage output |
| | ADC_VREF | I | SAR-ADC reference voltage input |

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|---|---|---|---|
| | SARADC_AIN[i] (i=0~7) | I | SAR-ADC input signal for 8 channel |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| ACODEC | HP_SENSE | I | The HP ground signal sense pin |
| | HPL_OUT | O | The HP left channel output pin |
| | HP_VGND | O | The HP virtual ground pin |
| | HPR_OUT | O | The HP right channel output pin |
| | LINEOUT_L | O | The Lineout Left channel output pin |
| | LINEOUT_R | O | The Lineout Right channel output pin |
| | VREF | O | The Codec IP reference voltage pin, should connect 1uf cap for stable |
| | MICBIAS_L | O | The Mic-phone left channel bias voltage pin |
| | MICBIAS_R | O | The Mic-phone right channel bias voltage pin |
| | MIC1P | I | The Mic-phone 1 differential input plus pin |
| | MIC1N | I | The Mic-phone 1 differential input minus pin |
| | IN1L | I | The Line-in 1 left channel input pin |
| | IN2L | I | The Line-in 2 left channel input pin |
| | MIC2N | I | The Mic-phone 2 differential input minus pin |
| | MIC2P | I | The Mic-phone 2 differential input plus pin |
| | IN1R | I | The Line-in 1 right channel input pin |
| | IN2R | I | The Line-in 2 right channel input pin |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| USB OTG 2.0 | USB_DM | I/O | USB OTG 2.0 Data signal DM |
| | USB_EXTR | N/A | Reference external resistance |
| | USB_DP | I/O | USB OTG 2.0 Data signal DP |
| | VBUS | N/A | USB OTG 2.0 5V power supply pin |
| | USB_ID | I | USB OTG 2.0 ID indicator |

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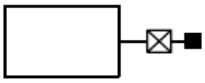
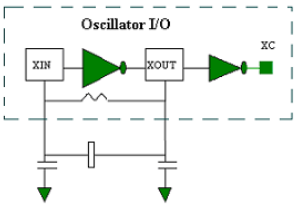
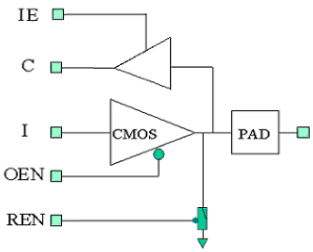
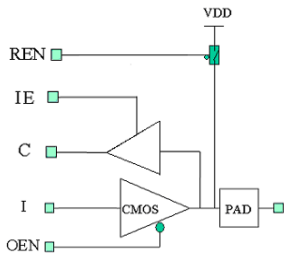
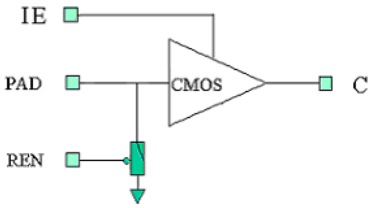
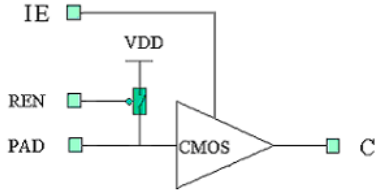
## 2.6 IO Type

The following list shows IO type except Power/Ground IO.

Table 2-3 RKNanoD IO Type List

| Type | Diagram | Description | Pin Name |
|---|---|---|---|
| A |  | Dedicated Power supply to Internal Macro with IO voltage | SARADC_AIN[2:0] |
| B |  | Crystal Oscillator with internal register | XIN24M/XOUT24M |
| C |  | CMOS 3-state output pad with controllable input and controllable pull-down | Part of digital GPIO (PBCDxRN) |
| D |  | CMOS 3-state output pad with controllable input and controllable pull-up | Part of digital GPIO (PBCUxRN) |
| E |  | controllable input pad with controllable pull-down | Part of digital GPIO (PICDRN) |
| F |  | controllable input pad with controllable pull-up | Part of digital GPIO (PICURN) |

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# Chapter 3 Electrical Specification

## 3.1 Absolute Maximum Ratings

Table 3-1 RKNanoD absolute maximum ratings

| Parameters | Max① | Unit |
|---|---|---|
| DC supply voltage for Internal digital logic | 1.32 | V |
| DC supply voltage for Digital GPIO (except for SAR-ADC, PLL, USB) | 3.6 | V |
| DC supply voltage for Analog part of SAR-ADC | 3.6 | V |
| DC supply voltage for Analog part of PLL | 3.3 | V |
| DC supply voltage for Analog part of USB OTG | 3.63 | V |
| Analog Input voltage for SAR-ADC | 2.75 | V |
| Analog Input voltage for DP/DM/VBUS of USB OTG | 5 | V |
| Digital input voltage for input buffer of GPIO | 3.6 | V |
| Digital output voltage for output buffer of GPIO | 3.6 | V |
| Storage Temperature | 150 | ℃ |

**Note:**

① Absolute maximum ratings would be update with real test after chip arrived.

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

## 3.2 Recommended Operating Conditions

Table 3-2 RKNanoD recommended operating conditions①

| Parameters | Min | Typ | Max | Units |
|---|---|---|---|---|
| Internal digital logic Power | 1.08 | 1.2 | 1.32 | V |
| Digital GPIO Power(3.3V) | 2.97 | 3.3 | 3.63 | V |
| PLL Analog Power | 2.97 | 3.3 | 3.63 | V |
| PLL Analog Power | 1.08 | 1.2 | 1.32 | V |
| SAR-ADC Analog Power | 2.97 | 3.3 | 3.63 | V |
| SAR-ADC external reference Power | 0.2* SAR_AVDD33 | | 0.9* SAR_AVDD33 | |
| USB OTG Analog Power(3.3V) | 2.97 | 3.3 | 3.63 | V |
| USB OTG external resistor | 40.5 | 45 | 49.5 | Ohm |
| Acodec Analog Power | 2.97 | 3.3 | 3.63 | V |
| PLL input clock frequency | N/A | 24 | N/A | MHz |
| Operating Temperature | -40 | 25 | 85 | ℃ |

**Note:**

① Recommended operating conditions update with real test after chip arrived.

## 3.3 DC Characteristics

Table 3-3 RKNanoD DC Characteristics

| Parameters | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Digital GPIO @3.3V | Input Low Voltage | Vil | -0.3 | 0 | 0.8 | V |
| | Input High Voltage | Vih | 2 | 3.3 | 3.6 | V |
| | Output Low Voltage | Vol | N/A | 0 | 0.4 | V |
| | Output High Voltage | Voh | 2.4 | 3.3 | N/A | V |
| | Threshold Point | Vt | 1.21 | 1.42 | 1.64 | V |

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|---|---|---|---|---|---|---|
| | Schmitt trig Low to High threshold point | Vt+ | 1.36 | 1.6 | 1.86 | V |
| | Schmitt trig High to Low threshold point | Vt- | 0.93 | 1.09 | 1.3 | V |
| | Pull-up Resistor | Rpu | 33 | 41 | 62 | K ohm |
| | Pull-down Resistor | Rpd | 33 | 42 | 68 | K ohm |
| Digital GPIO @1.8V | Input Low Voltage | Vil | -0.3 | 0 | 0.63 | V |
| | Input High Voltage | Vih | 1.17 | 1.8 | 2.1 | V |
| | Output Low Voltage | Vol | N/A | 0 | 0.45 | V |
| | Output High Voltage | Voh | 1.35 | 1.8 | N/A | V |
| | Threshold Point | Vt | 0.72 | 0.83 | 0.95 | V |
| | Schmitt trig Low to High threshold point | Vt+ | 0.74 | 0.88 | 1.03 | V |
| | Schmitt trig High to Low threshold point | Vt- | 0.52 | 0.61 | 0.73 | V |
| | Pull-up Resistor | Rpu | 67 | 93 | 152 | K ohm |
| | Pull-down Resistor | Rpd | 64 | 92 | 170 | K ohm |
| PLL | Input High Voltage | Vih_pll | 0.8*DVDD_iPLL (i=A,D,CG) | DVDD_iPLL (i=A,D,CG) | DVDD_iPLL (i=A,D,CG) | V |
| | Input Low Voltage | Vil_pll | 0 | 0 | 0.2*DVDD_iPLL (i=A,D,CG) | V |

## 3.4 Electrical Characteristics for General IO

Table 3-4 RKNanoD Electrical Characteristics for Digital General IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Digital GPIO @3.3V | Input leakage current | Il | Vin = 3.3V or 0V | -1 | N/A | 1 | uA |
| | Tri-state output leakage current | Ioz | Vout = 3.3V or 0V | -1 | N/A | 1 | uA |
| | High level input current | Iih | Vin = 3.3V, pull-down disabled | TBD | N/A | TBD | uA |
| | | | Vin = 3.3V, pull-down enabled | TBD | TBD | TBD | uA |
| | Low level input current | Iil | Vin = 0V, pull-up disabled | TBD | N/A | TBD | uA |
| | | | Vin = 0V, pull-up enabled | TBD | TBD | TBD | uA |
| Digital GPIO @1.8V | Input leakage current | Ii | Vin = 1.8V or 0V | -1 | N/A | 1 | uA |
| | Tri-state output leakage current | Ioz | Vout = 1.8V or 0V | -1 | N/A | 1 | uA |
| | High level input current | Iih | Vin = 1.8V, pull-down disabled | TBD | N/A | TBD | uA |
| | | | Vin = 1.8V, pull-down enabled | TBD | TBD | TBD | uA |
| | Low level input current | Iil | Vin = 0V, pull-up disabled | TBD | N/A | TBD | uA |
| | | | Vin = 0V, pull-up enabled | TBD | TBD | TBD | uA |

## 3.5 Electrical Characteristics for PLL

Table 3-5 RKNanoD Electrical Characteristics for PLL

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| PLL | Input clock frequency | Fin | Fin = FREF @3.3V/1.2V① | 1/10 | 24 | 800 | MHz |
| | Comparison frequency | Fref | FREF = Fin/REFDIV @3.3V/1.2V | 1 | N/A | 40 | MHz |
| | VCO operating range | Fvco | Fvco = Fref * FBDIV① @3.3V/1.2V | 400 | N/A | 1600 | MHz |
| | Output clock frequency | Fout | Fout = Fvco/POSTDIV① @3.3V/1.2V | 1 | N/A | 1600 | MHz |

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|---|---|---|---|---|---|---|---|
| | Lock time② | Tlt | @ 3.3V/1.2V, FREF=24M,REFDIV=1 | N/A | 41.7 | 62.5 | us |
| | VDDHV Power consumption ③ (normal mode) | N/A | Fvco = 1000MHz, @3.3V, 25 ℃ | N/A | 1 | 1.2 | mA |
| | VDD Power consumption (normal mode) | N/A | @3.3V/1.2V, 25 ℃ | N/A | 3 | 4 | uW/MHz |
| | Power consumption (bypass mode) | N/A | BYPASS=HIGH , PD= LOW , Fin = 24MHz, Fout = 24MHz, @3.3V/1.2V, 25 ℃ | N/A | N/A | N/A | uW |
| | Power consumption (power-down mode) | N/A | PD=HIGH, @27 ℃ | N/A | 10 | N/A | uA |

**Notes :**

① REFDIV is the input divider value; FBDIV is the feedback div POSTDIV is the output divider value ider value;
② Lock Time is 1000cycles of input clocks in typ, and 1500cycles of input clocks in max.
③ Current scale as (Fvco/1GHz)1.5

## 3.6 Electrical Characteristics for SAR-ADC

Table 3-6 RKNanoD Electrical Characteristics for SAR-ADC

| | Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| | ADC resolution | | | N/A | 10 | N/A | bits |
| | Conversion speed | Fs | | N/A | N/A | N/A | MSPS |
| | Differential Non Linearity | DNL | | N/A | N/A | N/A | LSB |
| | Integral Nn Linearity | INL | | N/A | N/A | N/A | LSB |
| | Gain Error | Egain | | N/A | N/A | N/A | %FS |
| | Offset Error | Eoffset | | N/A | N/A | N/A | %FS |
| | Input Range | CH[2:0] | 3-channel single-ended input | 0.01*SAR_AVDD33 | N/A | 0.99*SAR_AVDD33 | V |
| | Input Resistance | RIN | | N/A | N/A | N/A | Kom |
| | Input Capacitance | CIN | | N/A | 1 | N/A | pF |
| | Sampling Clock | | | N/A | 200 | N/A | KHz |
| | Main Clock Frequency | CLK | | N/A | 2.2 | N/A | MHz |
| | Data Latency | | | N/A | 11 | N/A | Clock Cycle |
| | SNR plus Distortion(Up to 5th harmonic) | SINAD | Fin=10K<br>Fin=99K | N/A | 61.49<br>60.58 | N/A | dB |
| | Spurious-Free Dynamic Range | SFDR | Fin=10K<br>Fin=99K | N/A | 66.29<br>67.14 | N/A | dB |
| | Second-Harmonic Distortion | 2HD | Fin=10K<br>Fin=99K | N/A | -72.64<br>-69.94 | N/A | dB |
| | Third-Harmonic Distortion | 3HD | Fin=10K<br>Fin=99K | N/A | -74.79<br>-68.85 | N/A | dB |
| | Effective Number of Bits | ENOB | Fin=10K<br>Fin=99K | N/A | 9.92<br>9.77 | N/A | Bits |
| | Positive Reference | VREF | | 0.2*SARADC_AVDD33 | | 0.9*SARADC_AVDD33 | V |
| | Analog Supply Current(SARADC_VDDA) | | | N/A | N/A | 200 | uA |
| | Digital Supply Current | | | N/A | N/A | 50 | uA |
| | Reference Supply Current | | | N/A | N/A | 50 | uA |
| | Power Down Current | | | N/A | N/A | N/A | uA |
| | Power up time | | | N/A | N/A | N/A | 1/Fs |

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## 3.7 Electrical Characteristics for USB Interface

Table 3-7 RKNanoD Electrical Characteristics for USB Interface

| Parameters | | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| HS transmit,(quiescent supply current; Vin=0 or 1) | Current From USB_AVDD33 | USB_AVDD33 = 3.3V<br>USB_DVDD12 = 1.2V | N/A | N/A | 0.1 | mA |
| | Current From USB_DVDD12 | | N/A | N/A | 20 | mA |
| Classic mode active(quiescent supply current; Vin=0 or 1) | Current From USB_AVDD33 | | N/A | N/A | 0.5 | mA |
| | Current From USB_DVDD12 | | N/A | N/A | 0.5 | mA |
| HS mode(CL=10pF) Active supply current | Current From USB_AVDD33 | | N/A | 0.1 | N/A | mA |
| | Current From USB_DVDD12 | | N/A | 2.22 | N/A | mA |
| FS transmit,(CL=50pF) Active supply current | Current From USB_AVDD33 | | N/A | 10 | 30 | mA |
| | Current From USB_DVDD12 | | N/A | 5 | 10 | mA |
| LS transmit(CL=50 to 350pF) Active supply current | Current From USB_AVDD33 | | N/A | 2 | 25 | mA |
| | Current From USB_DVDD12 | | N/A | 2 | 5 | mA |
| Suspend mode | Current From USB_AVDD33 | | N/A | N/A | 50 | uA |
| | Current From USB_DVDD12 | | N/A | N/A | 5 | uA |

## 3.8 Electrical Characteristics for Audio Codec Interface

Table 3-8 RKNanoD Electrical Characteristics for Audio Codec Interface

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Audio Codec | Full Scale Input Voltage<br>Line Input | N/A | | 1 | N/A | N/A | Vrms |
| | Full Scale Input Voltage<br>Mic Input (signal) | N/A | | 0.5 | N/A | N/A | Vrms |
| | Full Scale Input Voltage<br>Mic Input (differential) | N/A | | 1 | N/A | N/A | Vrms |
| | Full Scale Output Voltage<br>HP (for 10Kohm Loading) | N/A | | N/A | 1 | N/A | Vpeak |
| | Full Scale Output Voltage<br>HP (for 32ohm Loading) | N/A | | N/A | 0.8 | N/A | Vpeak |
| | Full Scale Output Voltage<br>HP (for 16ohm Loading) | N/A | | N/A | 0.8 | N/A | Vpeak |
| | S/N Ratio<br>Stereo DAC to HP with 10k/32/16 ohm loading | N/A | With A-weight Filter | | 100 | 102 | dB |
| | S/N Ratio<br>Stereo DAC to Line Out with 10k ohm loading | N/A | With A-weight Filter | | 100 | 102 | dB |
| | S/N Ratio<br>Line in to Stereo ADC | N/A | With A-weight Filter | N/A | 94 | N/A | dB |
| Audio Codec | S/N Ratio<br>Mic in to Stereo ADC with 0db gain (single end) | N/A | With A-weight Filter | N/A | 88 | N/A | dB |
| | S/N Ratio<br>Mic in to Stereo ADC with 0db signal (differential end) | N/A | With A-weight Filter | N/A | 94 | N/A | dB |
| | Total Harmonic Distortion + Noise<br>Stereo DAC to HP | N/A | | N/A | 83 | N/A | dB |
| | Total Harmonic Distortion + Noise<br>Stereo DAC to Line Out | N/A | | N/A | 85 | N/A | dB |
| | Total Harmonic Distortion + Noise<br>Line in to Stereo ADC | N/A | | N/A | 78 | N/A | dB |
| | Total Harmonic Distortion + Noise<br>Mic to Stereo ADC with 0db gain (differential or single end) | N/A | | N/A | 78 | N/A | dB |

PRELIMINARY

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | Power Consumption<br>All Power Down | N/A | | N/A | N/A | 100 | uW |
| | Power Consumption<br>Stereo DAC to HP with 10K/32/16 ohm loading | N/A | HP Power output 1mW | N/A | N/A | 15 | mW |
| | Power Consumption<br>Line in to Stereo ADC | N/A | | N/A | N/A | 14 | mW |
| | Power Down Current<br>IAVDD | N/A | | N/A | N/A | 2 | uA |
| | Power Down Current<br>IAVDD_IO | N/A | | N/A | N/A | 2 | uA |
| | MicBias Output Voltage | N/A | | 1.5 | N/A | AVDD | V |
| | MicBias Drive Current | N/A | | N/A | 4 | N/A | mA |

PRELIMINARY

# Chapter 4 Thermal Management

## 4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RKNanoD has to be below 85℃.

## 4.2 Package Thermal Characteristics

TBD

PRELIMINARY